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09/418,663	10/14/1999	James Robert Howard Hakewill	ARGONA.001A	9183

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EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/418,663	HAKEWILL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION-Non-Final

Introduction

1. Title is: METHOD AND APPARATUS FOR MANAGING THE CONFIGURATION AND FUNCTIONALITY OF A SEMICONDUCTOR DESIGN.

2. Applicants are: HAKEWILL et al.

3. Claims 1-51 were submitted on 10/14/99, and Claims 52-74 were added by preliminary amendment on 3/13/02.

4. Thus, Claims 1-74 have been submitted, examined, and rejected.

5. This is the first office action on the merits, and is non-final.

Response to Applicant's Remarks from Preliminary Amendment

6. Applicant's preliminary amendment includes Remarks on Page 9, which state that "new independent Claims 52, 53, 54, 55, 56, 57, 58, and 59 are generally analogous to existing independent Claims 1, 8, 35, 40, 46, 47, 49, and 51 respectively."

7. For convenience and clarity, the Examiner will refer to all the claims per their Page and line in the "REPLACEMENT CLAIMS" on Pages 31 through 41f of the preliminary amendment.

Index

8. **Dangelo'678** refers to Dangelo et al. US Patent 6,324,678 B1.

9. **Dupenloup'123** refers to Dupenloup et al. US Patent 6,378,123 B1.

10. **Wirthlin'434** refers to Wirthlin et al. US Patent 6,173,434.

11. **Dangelo'958** refers to Dangelo et al. US Patent 5,801,958.

12. **Rostoker'399** refers to Rostoker et al. US Patent 5,867,399.

13. **Cambell** refers to Cambell et al., "A tutorial for make", Proceedings of the 1985 ACM annual conference on the range of computing: mid-80's perpective, 1985, Denver, Colorado, United States. Pages 374-380. ISBN 0-89791-170-9.

14. **Gupte'474** refers to Gupte et al. US Patent 5,903,475.

15. **Heile'369** refers to Heile et al. US Patent 6,321, 369.

16. **Turino'892** refers to Turino et al. US Patent 5,994,892.

Priority claim acknowledged

17. **Acknowledgment is made of applicant's claim for priority** based on provisional patent application 60/104,271 filed Oct. 14, 1998.

Information Disclosure Statement- document #3 is illegible

18. The information disclosure statement filed 8/24/00 contains an illegible document. Specifically, document number 3, "Tuning a Customisable RISC Core for DSP" is not fully legible. The Examiner has read as much of this as possible (about 70%), but has put a line through the IDS to indicate that it was not fully legible. Please submit a fully legible copy.

Drawings-draftperson objection

19. **This application has been filed with informal drawings** which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Specifically, see the enclosed Form 948, Notice of Draftperson's Drawing Patent Review which objects to the drawings.

Specification-objections-informalities- Trademarks

20. **The disclosure is objected to because of the following informalities.** Appropriate correction is required.

21. At page 13 lines 14, a Trademark ("Wizard TM") is indefinitely mentioned. Please define this Trademarked component. Note MPEP 608.01(v) states "The relationship between a trademark and the product it identifies is sometimes indefinite, uncertain, and arbitrary. The formula or characteristics of the product may change from time to time and yet it may continue to be sold under the same trademark. In patent specifications, every element or ingredient of the product should be set forth in positive, exact, intelligible language, so that there will be no uncertainty as to what is meant. Arbitrary trademarks which are liable to mean different things at the pleasure of manufacturers do not constitute such language. Ex Parte Kattwinkle, 12 USPQ 11 (Bd. App. 1931)".

Claim Rejections - 35 USC § 112- first paragraph- enablement

22. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

23. **Claims 32, 61, 62, and 63 are rejected under 35 U.S.C. 112, first paragraph,** as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

24. Claim 32 states **"selecting a mathematical operation".**

25. Claim 61 states **"control logic".**

26. Claim 62 states **"instruction execution pipeline".**

27. Claim 63 states **"condition code choices"** and **"scratchpad RAM".**

28. The specification does not adequately describe these terms in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim Rejections - 35 USC § 112- fourth paragraph- further limitation

29. The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent forum shall contain a reference to a claim previously set fourth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

30. **Claims 38 and 39 are rejected under 35 U.S.C. 112, fourth paragraph,** as not specifying a further limitation of the subject matter claimed.

31. Begin by noting that Claim 35 is an "integrated circuit" by "method" claim **(product by process claim)** with 2 product limitations. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)".

32. **Claim 38 is rejected** because depends from Claim 35 (a product by process claim), with one additional process limitation that is not further limiting to the product (an integrated circuit).

33. This additional limitation is a process limitation: **"said method further comprises the act of selecting a process technology to be used for the design"** which does not further limit the product. Therefore, this additional process limitation is not a further limitation on the product, and is not a patentable difference. See MPEP 2113.

34. **Claim 39 is rejected** because depends from Claim 38 (a product by process claim), with one additional process limitation that is not further limiting to the product (an integrated circuit).

35. This additional limitation is a process limitation: **said process technology is a 0.18 micron process"** which does not further limit the product. Therefore, this additional process limitation is not a further limitation on the product, and is not a patentable difference. See MPEP 2113.

Claim Interpretation

36. Note, some of the claims have many limitations. The Examiner has taken the liberty of numbering these limitations for the sake of clarity.

Claim Rejections - 35 USC § 102(e)

37. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

38. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

39. Claims 1-6, 8, 10, 28-29, 31-32, 35, 38, 39, 50-54, 59 are rejected under 35 U.S.C. 102(e).

40. **Claim 1 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678

41. Claim 1 is an independent claim with 5 limitations.

42. **editing a first file specific to the design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

43. **defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

44. **generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

45. **running said script to create a customized description language model** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

46. **synthesizing said design based on said description language model** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

47. **Claim 2 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

48. Claim 2 depends from Claim 1, with one additional limitation.

49. **said description language comprises a hardware description language (HDL)** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

50. **Claim 3 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

51. Claim 3 depends from Claim 1, with one additional limitation.

52. **the act of synthesizing comprises running synthesis scripts based on said customized description language model** is disclosed by Dangelo'678 at Column 4 line 6 "separate programs are used to efficiently synthesize the different architectural blocks".

53. **Claim 4 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

54. Claim 4 depends from Claim 1, with one additional limitation.

55. **generating a second file for use with a simulation** is disclosed by Dangelo'678 at FIG 2 element 2 "DESIGN DESCRIPTION". Note that this design description element is part of an iterative loop, receiving feedback from element 6 "FUNCTIONAL VERIFICATION". Therefore, a second file, and perhaps many more files are generated as the design is iteratively modified.

56. **Claim 5 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

57. Claim 5 depends from Claim 4, with one additional limitation.

58. **evaluating the acceptability of the design based on said simulation** is disclosed by Dangelo'678 at FIG 2 element 6 "FUNCTIONAL VERIFICATION".

59. **Claim 6 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

60. Claim 6 depends from Claim 5, with one additional limitation.

61. **revising the design to produce a revised design, and re-synthesizing said revised design** is disclosed by Dangelo'678 at FIG 2 element 2 "DESIGN DESCRIPTION". Note that

this design description element is part of an iterative loop, receiving feedback from element 6 "FUNCTIONAL VERIFICATION".

62. **Claim 8 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678

63. Claim 8 is an independent claim with 4 limitations.

64. **editing a first file specific to said integrated circuit design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

65. **defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

66. generating a script using said first file, said library file, and user input information is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

67. **running said script to create said description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

68. **Claim 10 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

69. Claim 10 depends from Claim 8, with one additional limitation.

70. **said description language comprises VHDL** disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

71. **Claim 28 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

72. Claim 28 is an independent "method" claim with six limitations.

73. **providing a user with a plurality of optional instructions** is disclosed by Dangelo'678 at Column 28 line 55 "example of FIG. 17...pop up menu".

74. **selecting at least one of said plurality of optional instructions** is disclosed by Dangelo'678 at Column 28 line 58 "user has further selected one of the menu items".

75. **selecting at least one cache configuration** is disclosed by is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions".

76. **defining at least one memory interface** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

77. **generating a script based on said at least one optional instruction, cache configuration, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

78. **running said script to generate a hardware description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

79. **Claim 29 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

80. Claim 29 depends from Claim 28, with one additional limitation.

81. **selecting at least one synthesis library** is disclosed by Dangelo'678 at Column 12 line 16 "synthesis library".

82. **Claim 31 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

83. Claim 31 depends from Claim 28, with two additional limitations.

84. **synthesizing said design using said hardware description language model** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

85. **simulating said design using said hardware description language model** is disclosed by Dangelo'678 at Column 1 line 60 "generates a set of simulation results".

86. **Claim 32 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

87. Claim 32 depends from Claim 28, with one additional limitation.

88. optional instructions comprises selecting a mathematical operation to be performed on the data resident in at least one data register is disclosed by Dangelo'678 at Column 1 line 61 "instructions".

89. **Claim 35 is rejected** under 35 U.S.C. 102(e) as being anticipated by Rostoker'399.

90. Claim 35 is an independent claim. Additionally, Claim 35 is an "integrated circuit" by "method" claim (product by process claim) with 2 product limitations. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)".

91. **a microprocessor core** is disclosed by Rostoker'399 at Column 32 line 42 "microprocessor and/or memory core-cells".

92. **a memory operatively coupled to said microprocessor** is disclosed by Rostoker'399 at Column 32 line 42 "microprocessor and/or memory core-cells".

93. **Claim 38 is rejected** under 35 U.S.C. 102(e) as being anticipated by Rostoker'399.

94. Claim 38 depends from Claim 35 (a product by process claim), with one additional limitation.

95. This additional limitation is a process limitation: **"said method further comprises the act of selecting a process technology to be used for the design".**

96. Thus, Claim 38 is rejected for the same reasons as Claim 35. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)". Thus, the additional process limitation of Claim 38 is not a patentable difference.

97. **Claim 39 is rejected** under 35 U.S.C. 102(e) as being anticipated by Rostoker'399.

98. Claim 39 depends from Claim 38 (a product by process claim), with one additional limitation.

99. This additional limitation is merely a process limitation: **"said process technology is a 0.18 micron process".**

100. Thus, Claim 39 is rejected for the same reasons as Claim 38 and Claim 35. See MPEP 2113.

101. **Claim 50 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dupenloup'123.

102. Claim 50 is an independent "sub-micron feature integrated circuit" claim which is "synthesized by the following steps". This is a product by process claim with 2 product limitations. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)".

103. **microprocessor core having a program bus and data bus** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR and CONTROL BUS and DATA BUS.

104. **a random access memory (RAM) operatively coupled to said microprocessor** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM.

105. **Claim 51 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

106. Claim 51 is an independent "integrated circuit" claim which is "fabricated using the method". This is a product by process claim with 2 product limitations. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)".

107. **integrated circuit** is disclosed by Dangelo'678 at Column 24 line 4 "ASICs (Application Specific Integrated Circuits)".

108. **field programmable gate array FPGA** is disclosed by Dangelo'678 at Column 23 line 67 "memory modules (eg. ROM, EPROMS, FPGA).

109. **Claim 52 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

110. Claim 52 is an independent "method" claim with 4 limitations.

111. **obtaining user input information** is disclosed by Dangelo'678 at Column 1 line 63 "user input".

112. **identifying at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

113. **generating a script using at least said library file and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

114. **running said script to create a customized description language model** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

115. **Claim 53 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

116. Claim 53 is an independent "descriptive language model" claim with 4 limitations.

117. Claim 53 has substantially the same limitations as Claim 52, therefore is rejected for the same reasons.

118. **Claim 54 is rejected** under 35 U.S.C. 102(e) as being anticipated by Rostoker'399.

119. Claim 54 is an independent "integrated circuit" claim which is "designed using the method". This is a product by process claim with 2 product limitations. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)".

120. **a microprocessor core** is disclosed by Rostoker'399 at Column 32 line 42 "microprocessor and/or memory core-cells".

121. **a memory operatively coupled to said microprocessor** is disclosed by Rostoker'399 at Column 32 line 42 "microprocessor and/or memory core-cells".

122. **Claim 59 is rejected** under 35 U.S.C. 102(e) as being anticipated by Dangelo'678.

123. Claim 59 is an independent "integrated circuit" claim which is "designed using the method". This is a product by process claim with 1 product limitation. See MPEP 2113.

124. **integrated circuit** is disclosed by Dangelo'678 at Column 24 line 4 "ASICs (Application Specific Integrated Circuits)".

Claim Rejections - 35 USC § 103

125. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

126. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

127. Claims 7, 9, 11-27, 30, 33-34, 36-37, 40-49, 55-58, and 60-74 are rejected under 35 U.S.C. 103(a) as being unpatentable.

128. **Claim 7 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

129. Claim 7 depends from Claim 1, with three additional limitations.

130. **a cache configuration** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more randam access memories (RAM) 830").

131. **a memory interface configuration** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

132. Dangelo does not expressly disclose "custom instruction".

133. **at least one custom instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

134. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36.

135. **Claim 9 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

136. Claim 9 depends from Claim 8, with three additional limitations.

137. **(i)a cache configuration** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more randam access memories (RAM) 830").

138. **(ii)a memory interface configuration** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

139. Dangelo does not expressly disclose "custom instruction".

140. **(iii)at least one custom instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

141. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would

have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36.

142. **Claim 11 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434 and Dangelo'958.

143. Claim 11 depends from Claim 9, with one additional limitation.

144. selecting each of said plurality of parameters from a plurality of options presented by a menu-driven computer program

145. is disclosed by Dangelo'958 at Column 10 line 45 "user input occurs by pointing with the pointing device and selecting connection nodes, nets or devices and issuing commands which affect the selected object's numerical parameters".

146. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Dangelo'958 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36 and to select parameters quickly and efficiently.

147. **Claim 12 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

148. Claim 12 is in independent claim with 8 limitations.

149. **editing a first file specific to a desired integrated circuit design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

150. defining the location of at least one library file is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

151. **generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

152. running said script to create a customized description language model is disclosed by Dangelo at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

153. **generating a netlist which is descriptive of the circuitry of said integrated circuit** is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".

154. compiling said netlist and said hardware description model to produce a compiled integrated circuit design is disclosed by Dangelo'678 at Column 49 line 56 "compiling and simulating the netlist".

155. fabricating at least one mask representing said compiled integrated circuit design is disclosed by Dangelo'678 at Column 41 line 59 "mask level".

156. Dangelo'678 does not expressly disclose "fabricating said integrated circuit using said at least one mask".

157. fabricating said integrated circuit using said at least one mask is disclosed by Dupenloup'123 at Column 79 line 66 "wafer corresponding to the pattern on the mask".

158. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenlup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this fabricate the design that Dangelo'678 produced.

159. **Claim 13 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

160. Claim 13 depends from Claim 12, with four additional limitations.

161. **(ii)cache configurations** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more randam access memories (RAM) 830").

162. **(iii)memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

163. **(iv)system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

164. Dangelo'678 does not expressly disclose custom instruction sets.

165. (i)custom instruction sets is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

166. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to fabricate the design that Dangelo'678 produced.

167. **Claim 14 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

168. Claim 14 depends from Claim 12, one additional limitations.

169. **generating a list of logic devices and their interconnections** is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".

170. **Claim 15 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

171. Claim 15 depends from Claim 12, with one additional limitation.

172. Dangelo does not expressly disclose lithographic process.

173. **defining physical features on a semi-conductive substrate via a lithographic process** is disclosed by Dupenloup'123 at Column 79 line 58 to Column 80 line 1 "Photolithography...semiconductor material".

174. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678 produced.

175. **Claim 16 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

176. Claim 16 depends from Claim 12, with one additional limitation.

177. **synthesizing said design based on said description language model** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

178. **Claim 17 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Dangelo'958.

179. Claim 17 depends from Claim 13, with one additional limitation.

180. **editing is performed interactively with the user using a display** is disclosed by Dangelo'958 at Column 10 line 45 "user input occurs by pointing with the pointing device and

selecting connection nodes, nets or devices and issuing commands which affect the selected object's numerical parameters".

181. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Dangelo'958 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678 produced, and to facilitate the user interaction with the editing program.

182. **Claim 18 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

183. Claim 18 is an independent "apparatus" claim with 7 limitations.

184. **editing a first file specific to said integrated circuit design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

185. **defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

186. **generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

187. **running said script to create said description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

188. Dangelo'678 does not expressly disclose processor, storage device, and input device.

189. **a processor capable of running a computer program** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.

190. **a storage device being capable of storing at least a portion of a computer program** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

191. **an input device, operatively coupled to said processor, capable of receiving input from a user and transmitting said input to said processor** is disclosed by Dupenloup'123 at FIG 46 element 964 INPUT DEVICE.

192. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would

have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

193. **Claim 19 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

194. Claim 19 depends from Claim 18, with one additional limitation.

195. said description language model is a hardware description language (HDL) is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

196. **Claim 20 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

197. Claim 20 depends from Claim 18, with two additional limitations.

198. **generating a second file based on said description language model for use with a simulation** is disclosed by Dangelo'678 at Column 1 line 53 "information necessary for layout, verification and simulation into a schematic object file or files".

199. simulating said design using said second file is disclosed by Dangelo'678 at Column 1 line 61 "generates a set of simulation results".

200. **Claim 21 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

201. Claim 21 depends from Claim 20, with one additional limitation.

202. running synthesis scripts based on said description language model in order to synthesize said integrated circuit design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

203. **Claim 22 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

204. Claim 22 depends from Claim 18, with two additional limitations.

205. Dangelo'678 does not expressly disclose digital microprocessor and magnetic media storage device.

206. **said processor comprises a digital microprocessor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.

207. **said storage device comprises magnetic media** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

208. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

209. **Claim 23 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

210. Claim 23 is an independent "system" claim with six limitations.

211. **a first file comprising at least one instruction** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

212. **a second file comprising a plurality of cache configurations** is disclosed by is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions.

213. **a third file comprising a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

214. a second algorithm capable of generating a script based on selections made by said user from said first, second, and third files and

215. **input to said computer program via said input device** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

216. **a third algorithm capable of running said script to generate a description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

217. Dangelo'678 does not expressly disclose a computer having a processor and an input device.

218. **a computer having a processor and an input device** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR and element 964 INPUT DEVICE.

219. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

220. **Claim 24 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Rostoker'399.

221. Claim 24 depends from Claim 23, with two additional limitations.

222. Dangelo'678 does not expressly disclose object code and storage device.

223. **said program is embodied in object code** is disclosed by Rostoker'399

224. **stored on a storage device accessible by said processor** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

225. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 and Rostoker'399 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

226. **Claim 25 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Rostoker'399.

227. Claim 25 depends from Claim 24, with one additional limitation.

228. Dangelo'678 does not expressly disclose "rotating media magnetic storage device".

229. **rotating media magnetic storage device** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE and Column 76 line 40 "such as a disk drive unit".

230. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 and Rostoker'399 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

231. **Claim 26 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

232. Claim 26 depends from Claim 23, with one additional limitation.

233. **fourth file comprising a plurality of system architectures** is disclosed by Dangelo'678 at Column 2 line 31 "VHDS supports three distinct styles for the description of hardware architectures".

234. **Claim 27 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

235. Claim 27 depends from Claim 23, with one additional limitation.

236. **fourth algorithm capable of simulating said integrated circuit design based on said description language model** is disclosed by Dangelo'678 at Column 1 line 47 "logic simulator".

237. **Claim 30 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

238. Claim 30 depends from Claim 28, with one additional limitation.

239. **allowing the user to generate a customized optional instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

240. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36.

241. **Claim 33 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Cambell.

242. Claim 33 depends from Claim 31, with one additional limitation.

243. Dangelo'678 does not expressly disclose "makefile".

244. **simulating said design comprises generating a makefile** is disclosed by Cambell at Page 374 first paragraph "UNIX provides 'make', a program writing tool. It creates an executable up-to-date version of a program that consists of a variety of files which may require different treatments".

245. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Cambell to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to "split a very large program into small, relatively meaningful,

manageable modules by providing automatic compiling and linking" according to Cambell at Page 374 first paragraph.

246. **Claim 34 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte.

247. Claim 34 depends from Claim 28, with one additional limitation.

248. Dangelo'678 does not expressly disclose "selecting a process technology as the basis for the design"

249. selecting a process technology as the basis for the design is disclosed by Gupte at Column 4 line 60 "process technology".

250. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte

251. to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to save time and money by using the same circuit design methods for different process technologies.

252. **Claim 36 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Rostoker'399 in view of Heile'369.

253. Claim 36 depends from Claim 35, with one additional limitation.

254. **a digital signal processor (DSP) core** is disclosed by Heile'369 "complex megafunctions (i.e., off the shelf design blocks such as processors, DSP functions, bus controllers and interfaces)".

255. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Heile'369

256. to modify Rostoker'399. One of ordinary skill in the art would have been motivated to do this to save time and money and power and space by placing multiple functions in a single integrated circuit.

257. **Claim 37 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Rostoker'399 in view of Dupenloup'123.

258. Claim 37 depends from Claim 35, with two additional limitations.

259. **cache size is a non-zero number of bytes** is disclosed by Rostoker'399 at Column 32 line 42 "microprocessor and/or memory core-cells". Note that caches are a well known type of memory, and therefore are disclosed by Rostoker'399.

260. **said memory interface configuration defines at least one byte of random access memory space** is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit chip...functional circuit blocks...random access memories (RAM) 830 and an input/output (I/O) interface unit 831...macroblocks...modules".

261. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123

262. to modify Rostoker'399. One of ordinary skill in the art would have been motivated to do this to save time and money and power and space by placing multiple functions in a single integrated circuit.

263. **Claim 40 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

264. Claim 40 is an independent "system" claim (or "machine" per 35 USC 101), with 8 limitations.

265. **4-(ii) a plurality of cache configurations** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

266. **5-(iii) a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

267. Dangelo does not expressly disclose "custom instruction".

268. **6-(iv) a plurality of system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

269. 7-a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

270. **8-a second algorithm capable of running said script to generate a description language model of an integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

271. Dangelo'678 does not expressly disclose limitations 1-3.

272. **1-a processor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR

273. **2-a storage device in data communication with said processor** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM.

274. **3-(i) a plurality of custom instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

275. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36.

276. **Claim 41 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and Gupte.

277. Claim 41 depends from Claim 40, with one additional limitation.

278. Dangelo'678 does not expressly disclose the additional limitation.

279. **plurality of process technology options** is disclosed by Gupte at Column 4 line 60 "process technology".

280. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according

to Wirthlin'434 at Column 10 line 36, and to do this to save time and money by using the same circuit design methods for different process technologies.

281. **Claim 42 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and official notice (and mere automation).

282. Claim 42 depends from Claim 40, with one additional limitation.

283. Dangelo'678 does not expressly disclose the additional limitation.

284. **pre-configured data file** is disclosed by official notice that it is well known in the art to store the detailed parameters of user selected elements in pre-configured data files.

285. Also, using pre-configured data files is **merely automating** the manual entry of said data. In re Venner, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art."

286. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and official notice of data files to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to allow the user to quickly and accurately input large amounts of data in the form of pre-configured data files.

287. **Claim 43 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

288. Claim 43 is an independent "data storage device" claim (or "manufacture" per 35 USC 101), with 5 limitations.

289. **at least one functional instruction** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

290. **a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

291. **generating a script based on selections made by said user from said first and second files** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

292. running said script to generate a description language model of said integrated circuit design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

293. Dangelo'678 does not expressly disclose two of the limitations.

294. **data storage media** is disclosed by Dupenloup'123 FIG 46 element 968 MASS STORAGE.

295. **data storage media capable of storing a plurality of data bytes** is disclosed by Dupenloup'123 FIG 46 element 968 MASS STORAGE.

296. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the data storage media of Dupenloup'123.

297. **Claim 44 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and official notice.

298. Claim 44 depends from Claim 43, with 2 additional limitations.

299. Dangelo'678 does not expressly disclose the additional limitations.

300. **rotating magnetic disk** is disclosed by official notice that rotating magnetic disks are well known in the art. For example, floppy disks and hard drives are well known.

301. object code stored on said storage media is disclosed by official notice that object code is well known in the art. For example, the object oriented language "C+" is well known.

302. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and official notice to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the data storage media of Dupenloup'123, and using well known rotating magnetic disks and well known object codes.

303. **Claim 45 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Rostoker'399 and Gupte.

304. Claim 45 depends from Claim 43, with 3 additional limitations.

305. **a fourth file comprising a plurality of system architectures** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

306. Dangelo'678 does not expressly disclose two of the limitations.

307. **a third file comprising a plurality of cache configurations** is disclosed by Rostoker'399 at Column 32 line 42 "microprocessor and/or memory core-cells". Note that caches are a well known type of memory, and therefore are disclosed by Rostoker'399.

308. a fifth file comprising a plurality of process technology options is disclosed by Gupte at Column 4 line 60 "process technology".

309. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Rostoker'399 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the data storage media of Dupenloup'123 in order to store data, the "architecture synthesis system" to save money by allowing the same program to apply to various system architectures, and to store various memory configurations in a library of core-cells for quick selection, and to save money by allow the same program to design for various process technologies.

310. **Claim 46 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

311. Claim 46 is an independent "data storage device" claim with substantially the same limitations as "system" Claim 40. Therefore Claim 46 is rejected for the same reasons as Claim 40.

312. **Claim 47 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

313. Claim 47 is an independent "method" claim with 9 limitations.

314. **3-(ii) cache configuration** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

315. **4-(iii) memory interface configuration** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

316. **5-(iv) system architecture configuration** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

317. 6-defining the location of at least one library file is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

318. **7-generating a script using said first file and said library** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

319. 8-running said script to create a customized hardware description language model of the design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

320. **9-running a synthesis algorithm to synthesize a file descriptive of said design** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

321. Dangelo'678 does not expressly disclose 2 of the limitations.

322. **1-selecting a process technology** is disclosed by Gupte at Column 4 line 60 "process technology".

323. 2-(i) processor instructions is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

324. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to use Gupte to save time and money by using the same design program for various technologies, and to use Wirthlin'434 to save time by customizing the clock cycles to match the level of complexity of the instructions.

325. **Claim 48 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

326. Claim 48 is an independent "means for" claim with substantially the same limitations as Claim 40, thus is rejected for the same reasons.

327. **Claim 49 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dupenloup'123 in view of Gupte.

328. Claim 49 is an independent "sub-micron feature integrated circuit" which is "synthesized by the following steps". This is a product by process claim with 3 product limitations. Note that MPEP 2113 states "patentability is based on the product itself...In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964,966 (Fed. Cir. 1985)".

329. **1-microprocessor core having a program bus and data bus** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR and CONTROL BUS and DATA BUS.

330. **3-a random access memory (RAM) operatively coupled to said microprocessor** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM.

331. Dupenloup'123 does not expressly disclose one limitation.

332. **2-at least one cache memory** is disclosed by Gupte at Column 6 line 18 "cache memory".

333. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte to modify Dupenloup'123. One of ordinary skill in the art would have been motivated to use Gupte to increase the overall circuit performance speed by inserting a cache memory as a buffer.

334. **Claim 55 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and Gupte. Claim 55 is an independent "system for generating integrated circuit designs" claim, with 8 limitations

335. **5-(iii) a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

336. **6-(iv) a plurality of system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

337. **7-generating a script based on selections made by a user** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

338. **8- running said script to generate a description language model of an integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE

programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

339. Dangelo'678 does not expressly disclose 4 of the limitations:

340. **1-a processor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.

341. **2-a storage device in data communication with said processor** is disclosed by Dupenloup'123 at FIG 46 element 968 MASS STORAGE and element 956 RAM and CONTROL BUS and DATA BUS.

342. **3-(i) a plurality of custom instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

343. **4-(ii) a plurality of cache configurations** is disclosed by Gupte at Column 6 line 18 "cache memory".

344. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to use: Dupenloup'123 to implement the design method, Wirthlin'434 to customize the timing to allow complex instructions, and Gupte to increase the overall circuit performance speed by inserting a cache memory as a buffer.

345. **Claim 56 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and Gupte. Claim 56 is an independent "data storage device" claim, with 8 limitations that are substantially the same as Claim 55. Therefore, Claim 56 is rejected for the same reasons as Claim 55.

346. **Claim 57 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434 and Gupte. Claim 57 is an independent "method" claim with 8 limitations.

347. **4-(iii) memory interface configuration** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

348. **5-(iv) system architecture configuration** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

349. **6-identifying at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

350. **7-generating a script using said first data and said library** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

351. 8-running said script to create a customized hardware description language model of the design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

352. Dangelo'678 does not expressly disclose 3 limitations:

353. **1-selecting a process technology** is disclosed by Gupte at Column 4 line 60 "process technology".

354. **3-(ii) cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

355. 2-(i) processor instructions is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

356. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to select cache configurations and processor instructions in order to customize the process of Dangelo'678 to quickly and cheaply design alternate combinations of configurations and instructions, and to increase the overall circuit performance speed by inserting a cache memory as a buffer.

357. **Claim 58 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dupenloup'123 in view of Gupte. Claim 58 is an independent "sub-micron feature integrated circuit" product by process claim, with 3 product limitations. See MPEP 2113.

358. **microprocessor core having a program bus and data bus** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR and CONTROL BUS and DATA BUS.

359. **a random access memory (RAM) operatively coupled to said microprocessor** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM and CONTROL BUS and DATA BUS.

360. Dupenloup'123 does not expressly disclose "cache memory".

361. **at least one cache memory** is disclosed by Gupte at Column 6 line 18 "cache memory".

362. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte to modify Dupenloup'123. One of ordinary skill in the art would have been motivated to do this to increase the overall circuit performance speed by inserting a cache memory as a buffer.

363. **Claim 60 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

364. Claim 60 is an independent method claim with 2 limitations.

365. **generating a description of a hardware implementation of said configurable processor** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

366. Dangelo'678 does not expressly disclose one limitation:

367. **at least one user-defined instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

368. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

369. **Claim 61 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

370. Claim 61 depends from Claim 60, with one additional limitation.

371. Dangelo'678 does not expressly disclose the additional limitation:

372. **generating a description including control logic necessary for the execution of said at least one user-defined instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

373. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

374. **Claim 62 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

375. Claim 62 depends from Claim 61, with one additional limitation.

376. Dangelo'678 does not expressly disclose the additional limitation:

377. instruction execution pipeline having a plurality of stages, said control logic including portions associated with said

378. **stages** is disclosed by Dangelo'678 at Column 27 line 22 "specific control elements are assigned to the control logic in the RT level description of the system".

379. **Claim 63 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434 and Turino'892.

380. Claim 63 depends from Claim 60, with 3 additional limitations.

381. **(i)-registers** is disclosed by Dangelo'678 at Column 7 line 29 "registers".

382. **(iii)-scratchpad RAM** is disclosed by Dangelo'678 at Column 11 line 60 "RAM".

383. Dangelo does not disclose one limitation:

384. **(ii)-condition code choices** is disclosed by Turino'892 at Column

385. "Condition Code Register (CCR) - - 8 bits".

386. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Turino'892 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to minimize the number of bits in the condition code register.

387. **Claim 64 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

388. Claim 64 depends from Claim 60, with 1 additional limitation.

389. **at least one library of multimedia extensions** is disclosed by Dangelo'678 at Column 9 line 2 "libraries".

390. **Claim 65 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

391. Claim 65 depends from Claim 60, with 1 additional limitation.

392. **simulating said configurable processor** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

393. **Claim 66 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

394. Claim 66 depends from Claim 65, with 3 additional limitations.

395. **running at least one script to generate simulation data** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

396. **running at least one simulation using at least said simulation data** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

397. determining the adequacy of said configurable processor based at least in part on said act of running is disclosed by Dangelo'678 at Column 4 line 18 "This provides a check that the circuit implementation behaves as intended, and that the timing goals are achieved.

398. **Claim 67 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

399. Claim 67 depends from Claim 60, with 1 additional limitation.

400. synthesizing said configurable processor using at least said description is disclosed by Dangelo'678 at Column 4 line 6 "synthesis".

401. **Claim 68 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

402. Claim 68 depends from Claim 67, with 2 additional limitations.

403. **running at least one synthesis script to generate synthesis data** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

404. evaluating the adequacy of said synthesis data based at least in part on at least one design criterion is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

405. **Claim 69 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

406. Claim 69 depends from Claim 68, with 2 additional limitations.

407. at least one processor die size criterion is disclosed by Dangelo'678 at Column 41 line 46 "die size".

408. Dangelo'678 does not expressly disclose one limitation:

409. at least one specific processor performance criterion is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

410. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

411. **Claim 70 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

412. Claim 70 depends from Claim 68, with 3 additional limitations.

413. **revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

414. re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

415. and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

416. **Claim 71 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

417. Claim 71 depends from Claim 70, with 2 additional limitations.

418. **at least one processor die size criterion** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

419. **revising at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

420. **Claim 72 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

421. Claim 72 depends from Claim 71, with 2 additional limitations.

422. **at least one processor die size criterion** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

423. **revising at least one control file** is disclosed by Dangelo'678 at Column 27 line 22 "control elements".

424. **Claim 73 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

425. Claim 73 depends from Claim 70, with 2 additional limitations.

426. **processor clock speed** is disclosed by Dangelo'678 at Column 10 line 52 "length of clock cycle"

427. **at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

428. **Claim 74 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

429. Claim 74 depends from Claim 70, with 2 additional limitations.

430. **processor power consumption** is disclosed by Dangelo'678 Column 19 line 47 "allows the user to perform a "what if" analysis for choosing a preferred design in terms of size, speed, performance, technology, and power".

431. **at least one netlist (net load)** is disclosed by Dangelo'678 Column 49 line 56 "compiling and simulating the netlist".

Additional Cited Prior Art

432. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.

433. Gabele et al., US Patent 6,360,350 discloses "control file".

Conclusion

434. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.

435. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

436. (703) 746-7238 --- for communications after a Final Rejection has been made;

437. (703) 746-7239 --- for other official communications; and

438. (703) 746-7240 --- for non-official or draft communications.

439. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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